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EXAMINER	
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2622	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/675,960	SEKINE, HIROKAZU	
	Examiner	Art Unit	
	SELAM T. GEBRIEL	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5, 7-14, 16-21, and 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5, 7-14, 16-21, and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 07/18/2008 have been fully considered but they are not persuasive.

2. Claims 6, 15, and 22 are canceled.

3. As for argument, Hashimoto do not teach or suggest "a first and a second photoelectric conversion element, each of which corresponds to a pixel," as defined by amended Claim 1. As described at column 3, line 13, to column 4, line 48, of Hashimoto, the signals of photoelectric conversion portions a_{11} and a_{22} are added and input to one common amplifier connected to the corresponding vertical shift register V_0 connected to four adjacent pixels. Thus, each of the photoelectric conversion portions a_{11} and a_{22} do not correspond to a pixel (Remark, Page 11 Paragraph 2).

Examiner respectfully disagrees. The signal outputted form photoelectric conversion portion a_{11} corresponds to a pixel and the signal outputted from photoelectric conversion portion a_{22} corresponds to another pixel. See also Figure 4 the output of a_{11} + a_{12} or a_{21} + a_{22} can be added that is called a two **pixel** addition, since two pixels are added each photoelectric conversion corresponds to a pixel. See also Figure 5 where a_{11} corresponds to a green pixel, a_{12} corresponds to a red pixel, a_{21} corresponds to a blue pixel, and a_{22} corresponds to another green pixel.

4. As for argument, Hashimoto does not teach or suggest "the first and the second photoelectric conversion elements are spaced by ph0/2 and pv0/2 to each other in the horizontal and vertical directions," as recited by amended Claim 1, because Hashimoto does not provide a description of the spacing of the photoelectric conversion portions all and relative to predetermined pitches of unit cells (Remark, Page 11 Paragraph 3).

Examiner respectfully disagrees. Hashimoto teaches spacing of the photoelectric conversion portions all and relative to predetermined pitches of unit cells. See Figure 5 the spacing between a_{11} which corresponds to a (green or G) pixel and a_{21} corresponds to a (blue or B) pixel in the vertical direction. You can also say the same thing about the spacing between a_{11} which corresponds to a (green or G) pixel and a_{12} corresponds to a red pixel in horizontal direction.

Claim Objections

5. Claim 8 is objected to because of the following informalities: Claim 8 recites "A first and a second transfer transistor for transferring charges stored by the photoelectric conversion elements at their common floating **junctions. Junctions** should be replaced by **junction**. Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 1 recites the limitation "A first and second a transfer transistors for transferring charges stored by the photoelectric conversion elements to their common floating junction". **"The second transfer transistors"** lacks antecedent basis.

Claim 1 above and all the claims below are rejected under 112 because of the following reason. Applicant amended the claims but failed to follow up all changes or amendment in the following claims or limitations. For example applicant amended claim 1 Line 9 – 10 on page 2 as following "A first and a second transfer transistor for transferring charges stored by the photoelectric conversion elements to their **common floating junction** but applicant failed to amend claim 1 Line 16 - 18 on page 2, "Reset drain voltage lines provided in the column direction of the matrix arrangement for resetting the potential of **the common floating junctions** included in the unit cell belonging to each column of the matrix arrangement; It is now clear to the examiner whether there is a common floating **junction** or more than one common floating **Junctions**. Similar errors have been found in most of the claims and applicant is advised to check all the claims for similar errors.

Claim 1 recites the limitation "Second transfer lines in the row direction of the matrix arrangement for controlling **the second transfer transistors** included in the unit cells belonging to each row of the matrix arrangement". **"The second transfer transistors"** lacks antecedent basis.

Claim 1 recites the limitation "Signal output lines provided in the column direction of the matrix arrangement to which the output voltages of **the driver transistors**

included in the unit cells belonging to each column of the matrix arrangement are supplied". "**The driver transistors**" lacks antecedent basis.

Claim 1 recites the limitation "Address lines provided in the row direction of the matrix arrangement for selectively driving **the drives transistors** included in the unit cell belonging to each row". "**The driver transistors**" lacks antecedent basis.

Claim 4 recites the limitation "**The driver transistors** and **the address transistors** which are included in the respective unit cells are connected in series, wherein the first and second photoelectric conversion elements are connected to gate electrodes of **the driver transistors** via **the first and second transfer transistors**, and wherein source electrodes of **the reset transistors** are connected to the gate electrodes of **the driver transistors**". "**The driver transistors, the address transistors, and the reset transistors**" lacks antecedent basis.

Claim 7 recites the limitation "The unit cells are formed as an integrated circuit on a semiconductor substrate and the first and second photodiodes arranged in the oblique direction share the floating junction area, the reset drain area, **the reset transistors, the driver transistors, the address transistors**, the junction area between **the driver transistors** and **the address transistors** and the diffusion area at the connecting portion between **the driver transistors** and the signal output line, thereby reading signals of the first pixel row and the second pixel row independently". "**The driver transistors, the address transistors, and the reset transistors**" lacks antecedent basis.

Claim 8 recites the limitation “Reset drain voltage lines provided in the column direction of the matrix arrangement for resetting the potential of **the common floating junctions** included in the unit cell belonging to each column of the matrix arrangement”. **“The common floating junctions”** lacks antecedent basis.

Claim 8 recites the limitation “Second transfer lines in the row direction of the matrix arrangement for controlling **the second transfer transistors** included in the unit cells belonging to each row of the matrix arrangement”. **“The second transfer transistors"** lacks antecedent basis.

Claim 8 recites the limitation “Second transfer lines in the row direction of the matrix arrangement for controlling **the second transfer transistors** included in the unit cells belonging to each row of the matrix arrangement”. **“The second transfer transistors"** lacks antecedent basis.

Claim 8 recites the limitation “Second transfer lines in the row direction of the matrix arrangement for controlling **the second transfer transistors** included in the unit cells belonging to each row of the matrix arrangement”. **“The second transfer transistors"** lacks antecedent basis.

Claim 8 recites the limitation “Second transfer lines in the row direction of the matrix arrangement for controlling **the second transfer transistors** included in the unit cells belonging to each row of the matrix arrangement”. **“The second transfer transistors"** lacks antecedent basis.

Claim 8 recites the limitation “First signal output lines provided in the column direction of the matrix arrangement to which the output voltages of **the driver**

transistors included in the unit cells arranged in the odd numbered rows are supplied". "**The driver transistors**" lacks antecedent basis.

Claim 8 recites the limitation "Second signal output lines provided in the column direction of the matrix arrangement to which the output voltages of **the driver transistors** included in the unit cells arranged An the even numbered rows are supplied". **"The driver transistors"** lacks antecedent basis.

Claim 8 recites the limitation "Address lines provided in the row direction of the matrix arrangement for selectively driving **the driver transistors** included in the unit cell belonging to each row". **"The driver transistors"** Lacks antecedent basis.

Claim 9 recites limitation "wherein the adjacent pixel lines, which are read simultaneously, are a pixel row formed by **the second photoelectric conversion elements** included in the unit cell belonging to the first row and a pixel row formed by the first photoelectric conversion element included in the unit cell belonging to the second row, thereby simultaneously read the image signals of the pixel of adjacent tow rows into the first and second signal output lines by respectively supplying the same transfer pulse to the second transfer line provided for the unit cell belonging to the first row and the first transfer line provided for the unit cell belonging to the second row" . "**The second photoelectric conversion elements**" lacks antecedent basis.

Claim 13 recites limitation "wherein the driver transistors and the address transistors, which are included in the unit cells are connected in series, wherein the first and second photoelectric conversion elements are connected no gate electrodes of **the driver transistors** via the first and second transfer transistors, and wherein source

electrodes of **the reset transistors** are connected to the gate electrodes of **the driver transistors**". "**The reset transistors, and driver transistors"** lacks antecedent basis.

Claim 16 recites limitation "wherein the unit cells are formed as an integrated circuit on a semiconductor substrate and wherein the first and second photodiodes arranged in the oblique direction share the floating junction area, the reset drain area, **the reset transistors, the driver transistors, the address transistors**, the junction area between **the driver transistors** and **the address transistors,** and the diffusion area at the connecting portion between **the driver transistors** and the signal output line, thereby reading signals of the first pixel row and the second pixel row independently". "**The reset transistors, the address transistors and driver transistors"** lacks antecedent basis.

Claim 20 recites limitation "wherein the driver transistors and the address transistors which are included in the unit cells are connected in series, and the first and second photoelectric conversion elements are connected to gate electrodes of **the driver transistors** via the first and second transfer transistors, and source electrodes of **the reset transistors** are connected to the gate electrodes of **the driver transistors**". "**The reset transistors, the address transistors and driver transistors"** lacks antecedent basis.

Claim 23 recites limitation "wherein unit cells are formed as an integrated circuit on a semiconductor substrate and the first and second photodiodes arranged in the oblique direction share the floating junction area, the reset drain area, **the reset transistors, the driver transistors, the address transistors**, the junction area

between **the driver transistors** and **the address transistors**, and the diffusion area at the connecting portion between **the driver transistors** and the signal output line, thereby read signals of the first pixel row and the second pixel row independently". "**The reset transistors, the address transistors and driver transistors**" lacks antecedent basis.

Claim Rejections - 35 USC § 102

8. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

9. Claims 1 – 5, 7 – 14, 16 – 21, and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Hashimoto (US 6,956,605 B1).

10. Regarding claim 1, Hashimoto discloses a CMOS image sensor (Figure 2 and 19 - 22) comprising:

A plurality of unit cells (Figure 21, Element 81) arranged in the row and column directions at a predetermined pitches of pho and pvo respectively in a two-dimensional plain forming a matrix, (Col 13, Line 29 – 67 and see response to argument) each of the unit cells including:

A first and a second photoelectric conversion element each of which corresponds to a pixel (Figure 19- 22, Photo conversion elements a11, a22, a12, and a21, See Response to argument),

A first and a second transfer transistor (Figure 19, Amplifier portion 12 includes Transfer Means MTX3 and Transfer means MTX2 as shown in figure 2, See Col 13 Line 35 - 36) for transferring charges stored by the photoelectric conversion elements to their common floating junction (Col 13, Line 35 – 36 and Col 14, Line 1 – 65);

Reset transistor (Figure 19, Amplifier portion 12 includes Reset means MRES as shown in Figure 2, Col 13 line 35 – 36) for resetting the potential of the floating junction.

Driver transistor (Figure 19, , Amplifier portion 12 includes Reset means MSF as shown in Figure 2, Col 13 line 35 – 36) whose output potential is controlled by the potential of the floating junction, and

Address transistor (Figure 19, Amplifier portion 12 includes select means MSEL as shown in Figure 2, Col 13 line 35 – 36) for selectively driving the driver transistor;

Reset drain voltage lines (Figure 22, Reset Line112) provided in the column direction of the matrix arrangement for resetting the potential of the common floating junctions included in the unit cell belonging to each column of the matrix arrangement (Col 14 Line 50 – 60);

First transfer lines (Figure 22, Scanning lines 108a – 108d) provided in the row direction of the matrix arrangement for controlling the first transfer transistor included in the unit cell belonging to each row (See Figure 2, 19 – 22, Col 14 Line 50 – 60);

Second transfer lines (Figure 22, Scanning lines 108a – 108d) in the row direction of the matrix arrangement for controlling the second transfer transistors included in the unit cells belonging to each row of the matrix arrangement (See Figure 2, 19 – 22 , Col 14 Line 50 – 60);

Signal output lines (Figure 22, A Vertical signal Line 107) provided in the column direction of the matrix arrangement to which the output voltages of the driver transistors included in the unit cells belonging to each column of the matrix arrangement are supplied (See Figure 2, 19 – 22, Col 14 Line 50 – 60), and

Address lines (Figure 22, Row selection line 110) provided in the row direction of the matrix arrangement for selectively driving the drives transistors included in the unit cell belonging to each row (See Figure 2, 19 – 22 , Col 14 Line 50 – 60).

The first and the second photoelectric conversion elements are spaced by phO/2 and pvO/2 to each other in the horizontal and vertical directions, thereby being arranged in an oblique direction in relation to the row or column directions of the matrix (Col 4, Line 24 - 32, Col 4, Line 39 – 47 and Figure 4and 19 - 22 See also, Response to argument), and

The first and the second transfer transistors (Figure 19, Amplifier portion 12 includes Transfer Means MTX3 and Element MTX2 as shown in figure 2, See Col 13 Line 35 - 36), the floating junction, the reset transistor, the driver transistor or the address transistor included in each of the unit cells are placed in areas surrounded by adjacent unit cells (See Figure 2 and Figure 4).

11. Regarding claim 2, A CMOS image sensor according to Claim 1, wherein:

A first pixel line (Col 8, Line 60 – 67 to Col 9 Line 1 – 8) composed of the first photoelectric conversion element included in the unit cells belonging to each row of the

matrix arrangement (See Figure 2, 19 – 22 and Col 13, Line 59 – 67 to Col 14, Line 1 – 65) and

A second pixel lines (Col 8, Line 60 – 67 to Col 9 Line 1 – 8) composed of the second photoelectric conversion element included in the unit cells are independently read respectively by the first and second transfer lines (See Figure 2, 19 – 22 and Col 13, Line 59 – 67 to Col 14, Line 1 – 65).

12. Regarding claim 3, A CMOS image sensor according to Claim 2, wherein:

The first pixel lines and the second pixel lines (Col 8, Line 60 – 67 to Col 9 Line 1 – 8) are read by switching the first and second transfer transistors by the first and second transfer lines (See Figure 2, 19 – 22 and Col 13, Line 59 – 67 to Col 14, Line 1 – 65).

13. Regarding claim 4, A CMOS image sensor according to Claim 3, wherein:

The driver transistors (Figure 1, Amplification means MSF) and the address transistors (Figure 1, Select means MSEL) which are included in the respective unit cells are connected in series, wherein the first and second photoelectric conversion elements are connected to gate electrodes of the driver transistors via the first and second transfer transistors, and wherein source electrodes of the reset transistors are connected to the gate electrodes of the driver transistors (See Figure 2, Col 3 Line 43 - 63 and see Figure 21 and 22, Col 13, Line 59 – 67 to Col 14, Line 1 – 65).

14. Regarding claim 5, A CMOS image sensor according to Claim 4, wherein the first and second photoelectric conversion elements are photodiodes (Figure 21, Element 82a – 82d are photodiodes).

15. Regarding claim 7, A CMOS image sensor according to Claim 5, wherein:

The unit cells are formed as an integrated circuit on a semiconductor substrate (Col 12, Line 55 – 58) and

The first and second photodiodes arranged in the oblique direction share the floating junction area, the reset drain area, the reset transistors, the driver transistors, the address transistors, the junction area between the driver transistors and the address transistors and the diffusion area at the connecting portion between the driver transistors and the signal output line, thereby reading signals of the first pixel row and the second pixel row independently (See Figure 2 and Figure 21, Col 4, Line 39 – 47).

16. Regarding claim 8, A CMOS image sensor (Figure 2 and 19 - 22) Comprising:

A plurality of unit ceils (Figure 21, Element 81) arranged in the row and column directions at a predetermined pitch of pho and pv0 respectively in a two-dimensional plain forming a matrix, each of the unit cells including

A first and a second photoelectric conversion element each of which corresponds to a pixel (Figure 19- 22, Photo conversion elements a11, a22, a12, and a21, See Response to argument),

A first and a second transfer transistor (Figure 19, Amplifier portion 12 includes Transfer Means MTX3 and Transfer Means MTX2 as shown in figure 2, See Col 13 Line 35 - 36) for transferring charges stored by the photoelectric conversion elements to their common floating junction (Col 13, Line 35 – 36 and Col 14, Line 1 – 65);

Reset transistor (Figure 19, Amplifier portion 12 includes Reset means MRES as shown in Figure 2, Col 13 line 35 – 36) for resetting the potential of the floating junction,

Driver transistor (Figure 19, , Amplifier portion 12 includes Reset means MSF as shown in Figure 2, Col 13 line 35 – 36) whose output potential is controlled by the potential of the floating junction, and

Address transistor (Figure 19, Amplifier portion 12 includes select means MSEL as shown in Figure 2, Col 13 line 35 – 36) for selectively driving the driver transistor;

Reset drain voltage lines (Figure 22, Reset Lines 112) provided in the column direction of the matrix arrangement for resetting the potential of the common floating junctions included in the unit cell belonging to each column of the matrix arrangement (Col 13, Line 62 – 67);

First transfer lines (Figure 22, Scanning lines 108a – 108d) provided in the row direction of the matrix arrangement for controlling the first transfer transistor included in the unit cell belonging to each row (Col 13, Line 59 – 67 to Col 14, Line 1 – 65);

Second transfer lines (Figure 22, Scanning lines 108a – 108d) in the row direction of the matrix arrangement for controlling the second transfer transistors included in the unit cells belonging to each row of the matrix arrangement (Col 13, Line 59 – 67 to Col 14, Line 1 – 65);

First signal output lines (Figure 22, A Vertical signal Line 107) provided in the column direction of the matrix arrangement to which the output voltages of the driver transistors included in the unit cells arranged in the odd numbered rows are supplied (Col 8, Line 60 – 67 to Col 9 Line 1 – 8);

Second signal output lines (Figure 22, A Vertical signal Line 107) provided in the column direction of the matrix arrangement to which the output voltages of the driver transistors included in the unit cells arranged An the even numbered rows are supplied (Col 8, Line 60 – 67 to Col 9 Line 1 – 8); and

Address lines (Figure 22, Row selection line 110) provided in the row direction of the matrix arrangement for selectively driving the driver transistors included in the unit cell belonging to each row (Col 13, Line 59 – 67 to Col 14, Line 1 – 65);

The first and the second photoelectric conversion elements are spaced by phO/2 and pvO/2 to each other in the horizontal and vertical directions, thereby being arranged in an oblique direction in relation to the row or column directions of the matrix (Col 4, Line 24 - 32, Col 4, Line 39 – 47 and See Figure 2 and Figure 19 – 22, See also, Response to argument), and

The first and the second transfer transistors, the floating junction, the reset transistor, the driver transistor or the address transistor included in each of the unit cells are placed in areas surrounded by adjacent unit cells (See Figure 2 and Figure 19 – 22).

Wherein image signals of the pixel arrays composed of the photoelectric conversion elements included in the unit cells arranged in the neighboring two columns

are read simultaneously using the first and second signal output lines (Col 13, Line 59 – 67 to Col 14, Line 1 – 65).

17. Regarding claim 9, A CMOS image sensor according to Claim 8, wherein the adjacent pixel lines, which are read simultaneously, are a pixel row formed by the second photoelectric conversion elements included in the unit cell belonging to the first row and a pixel row formed by the first photoelectric conversion element included in the unit cell belonging to the second row, thereby simultaneously read the image signals of the pixel of adjacent tow rows into the first and second signal output lines by respectively supplying the same transfer pulse to the second transfer line provided for the unit cell belonging to the first row and the first transfer line provided for the unit cell belonging to the second row (See Figure 2, 19 – 22 and Col 13, Line 59 – 67 to Col 14, Line 1 – 65).

18. Regarding claim 10, A CMOS image sensor according to Claim 9,

A gate of the second transfer transistor included in the unit cell belong to the first row and a gate of the first transfer transistor included in the unit cell belong to the second row are connected to each other (See Figure 2, 19 – 22 Col 13, Line 59 – 67 to Col 14, Line 1 – 65).

19. Regarding claim 11, A CMOS image sensor according to Claim 10, wherein the first pixel row composed of the first photoelectric conversion element included in the unit

cells belonging to the respective rows of the matrix arrangement and the second pixel row composed of the second photoelectric conversion element included in the unit cells are independently read respectively by the first and second transfer lines (See Figure 2, 19 – 22 and Col 13, Line 59 – 67 to Col 14, Line 1 – 65).

20. Regarding claim 12, A CMOS image sensor accordin9 to Claim 11, wherein the first pixel row and the second pixel row are read by switching the first and second transfer transistors by the first and second transfer lines (See Figure 2, 19 – 22 and Col 13, Line 59 – 67 to Col 14, Line 1 – 65).

21. Regarding claim 13, A CMOS image sensor according to Claim 12, wherein the driver transistors and the address transistors, which are included in the unit cells are connected in series, wherein the first and second photoelectric conversion elements are connected no gate electrodes of the driver Transistors via the first and second transfer transistors, and wherein source electrodes of the reset transistors are connected to the gate electrodes of the driver transistors (See Figure 2, 19 – 22 and Col 13, Line 59 – 67 to Col 14, Line 1 – 65).

22. Regarding claim 14, A CMOS image sensor according to Claim 13, wherein the first and second photoelectric conversion elements are photodiode (Figure 21, Element 82a – 82d are photodiodes).

23. Regarding claim 16, ACMOS image sensor according to Claim 15, wherein the unit cells are formed as an integrated circuit on a semiconductor substrate and wherein the first and second photodiodes arranged in the oblique direction share the floating junction area, the reset drain area, the reset transistors, the driver transistors, the address transistors, the junction area between the driver transistors and the address transistors, and the diffusion area at the connecting portion between the driver transistors and the signal output line, thereby reading signals of the first pixel row and the second pixel row independently (See Figure 2, 19 – 22 and Col 13, Line 59 – 67 to Col 14, Line 1 – 65).

24. Regarding claim 17, A CMOS image sensor according to Claim 1, wherein among unit cells arranged in adjacent two rows of the matrix arrangement, a gate of the address transistor included in the unit cell arranged in the first row and a gate of the reset transistor included in the unit cell arranged in the second row are connected, and while an image signal from the second photoelectric conversion element included in the unit arranged in the first row is being read, the floating junction included in the unit cell arranged in the second row to be read next is reset, thus an image signal from the first photoelectric conversion element included in the unit cell arranged in the second row can be read (See Figure 2, 19 – 22 and Col 13, Line 59 – 67 to Col 14, Line 1 – 65).

25. Regarding claim 18, A CMOS image sensor according to Claim 17, wherein a first pixel row composed of the first photoelectric conversion element included in the unit

cell belonging to each row of the matrix arrangement and a second pixel row composed of the second photoelectric conversion element included in the unit cell are independently read by the first and second transfer lines (See Figure 2, 19 – 22 and Col 13, Line 59 – 67 to Col 14, Line 1 – 65).

26. Regarding claim 19, A CMOS image sensor according to Claim 18, wherein the first pixel row and the second pixel row are read by switching the first and second transfer transistors by the first and second transfer lines (See Figure 2, 19 – 22 and Col 8, Line 60 – 67 to Col 9 Line 1 – 8, Col 13, Line 59 – 67 to Col 14, Line 1 – 65).

27. Regarding claim 20, A CMOS image sensor according to Claim 19, wherein the driver transistors and the address transistors which are included in the unit cells are connected in series, and the first and second photoelectric conversion elements are connected to gate electrodes of the driver transistors via the first and second transfer transistors, and source electrodes of the reset transistors are connected to the gate electrodes of the driver transistors (See Figure 2, 19 – 22 and Col 13, Line 59 – 67 to Col 14, Line 1 – 65).

28. Regarding claim 21, A CMOS image sensor according to Claim 19, wherein the first and second photoelectric conversion elements are photodiodes (Figure 21, Element 82a – 82d are photodiodes).

29. Regarding claim 23, A CMOS image sensor according to Claim 21, wherein unit cells are formed as an integrated circuit on a semiconductor substrate and the first and second photodiodes arranged in the oblique direction share the floating junction area, the reset drain area, the reset transistors, the driver transistors, the address transistors, the junction area between the driver transistors and the address transistors, and the diffusion area at the connecting portion between the driver transistors and the signal output line, thereby read signals of the first pixel row and the second pixel row independently (See Figure 2, 19 – 22 and Col 13, Line 59 – 67 to Col 14, Line 1 – 65).

Conclusion

1. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SELAM T. GEBRIEL whose telephone number is (571)270-1652. The examiner can normally be reached on Monday-Thursday 7.30am-5.00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tran Sinh can be reached on 571-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tuan V Ho/
Primary Examiner, Art Unit 2622
/S. T. G./
Examiner, Art Unit 2622

Tuesday, October 28, 2008